FIG.1

ENTIRE BLOCK DIAGRAM OF A NONVOLATILE SEMICONDUCTOR MEMORY DEVICE ACCORDING TO A FIRST EMBODIMENT

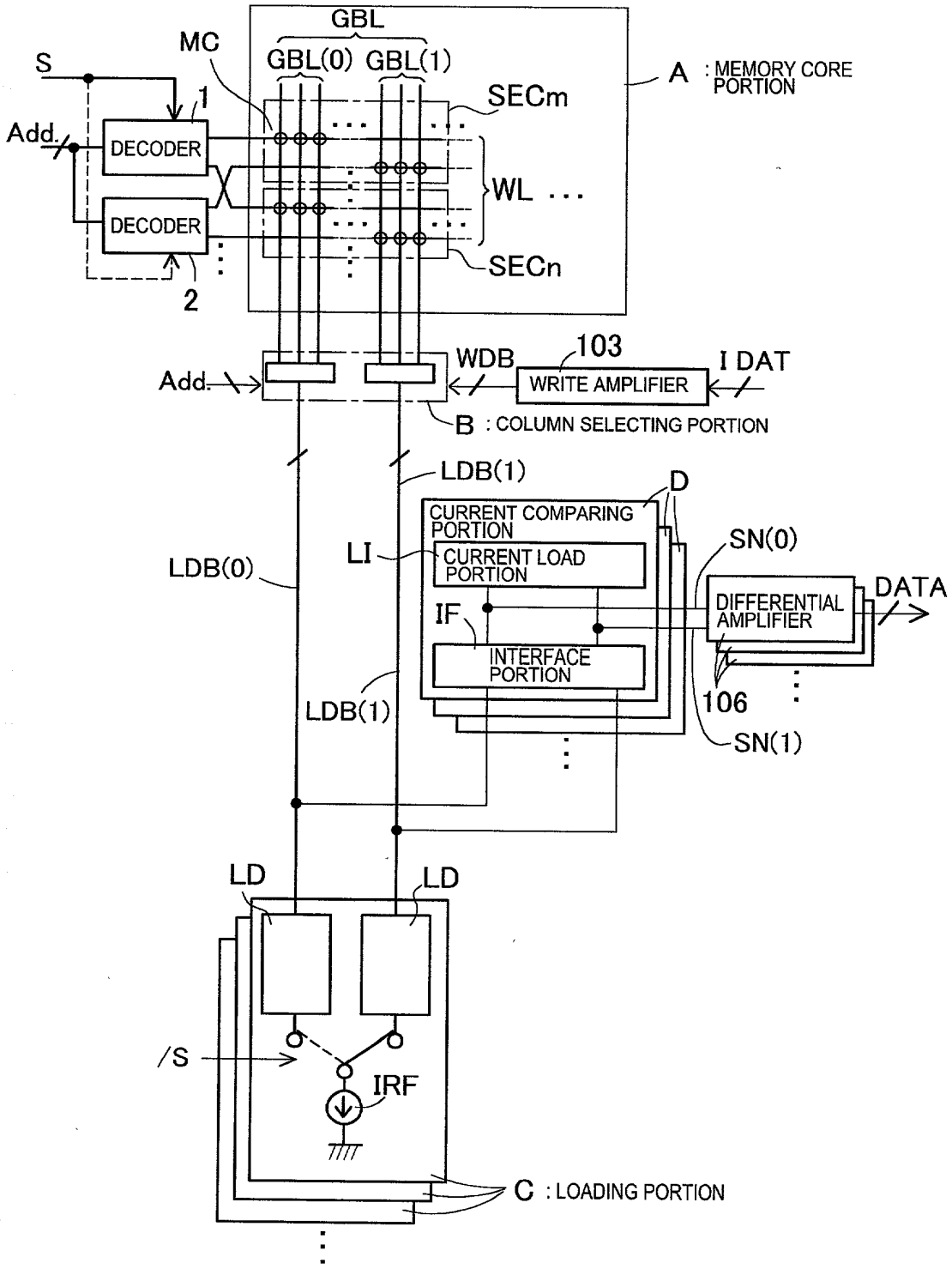


FIG.2

CIRCUIT DIAGRAM SHOWING A THEORETICAL BLOCK DIAGRAM OF A MEMORY CORE PORTION OF THE FIRST EMBODIMENT

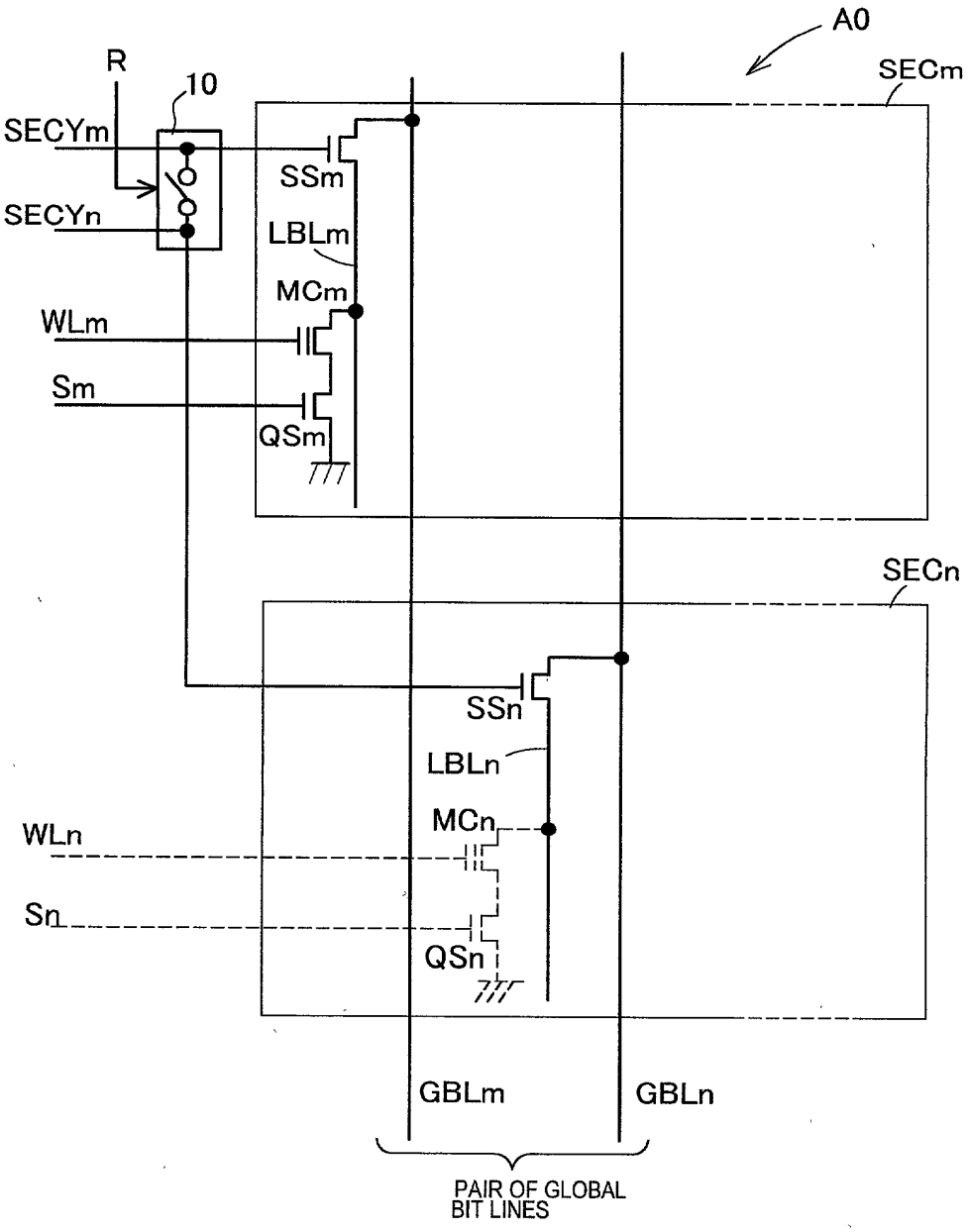


FIG.3

CIRCUIT DIAGRAM SHOWING A FIRST EXAMPLE OF THE MEMORY CORE PORTION

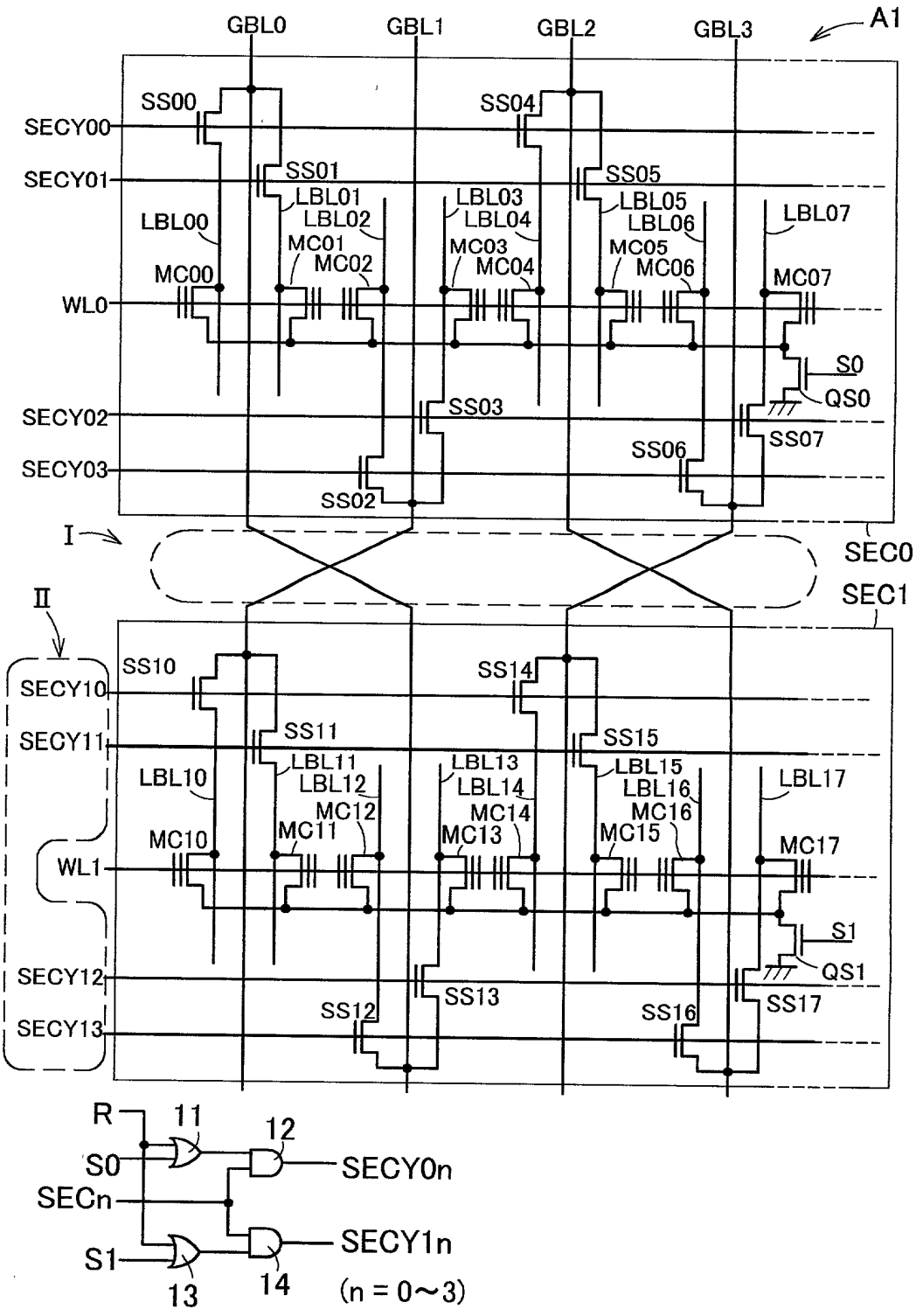


FIG.4

CIRCUIT DIAGRAM SHOWING A SECOND EXAMPLE OF THE MEMORY CORE PORTION

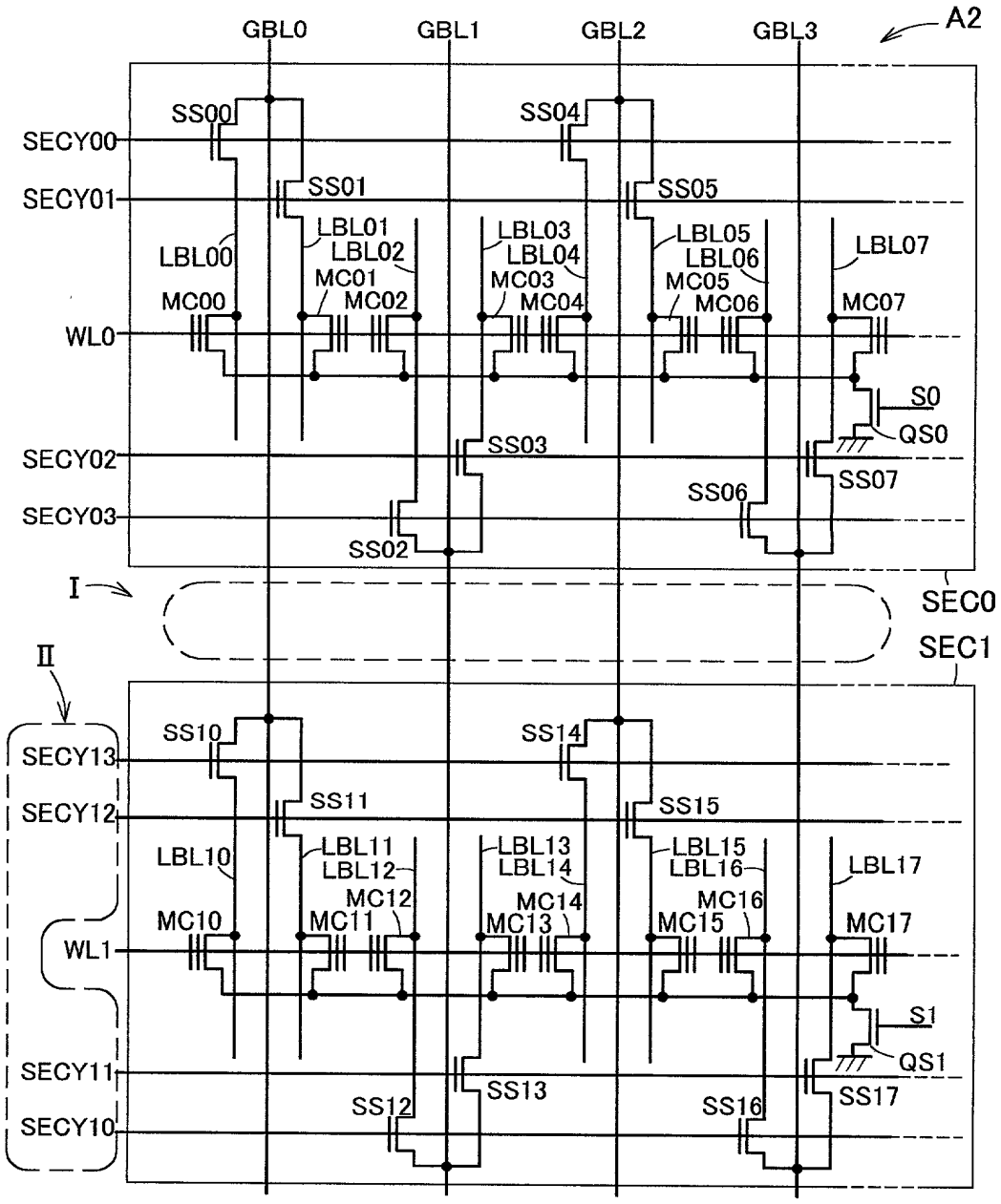


FIG.5

CIRCUIT DIAGRAM SHOWING REDUNDANT STRUCTURES OF THE FIRST AND SECOND EXAMPLES OF THE MEMORY CORE PORTION

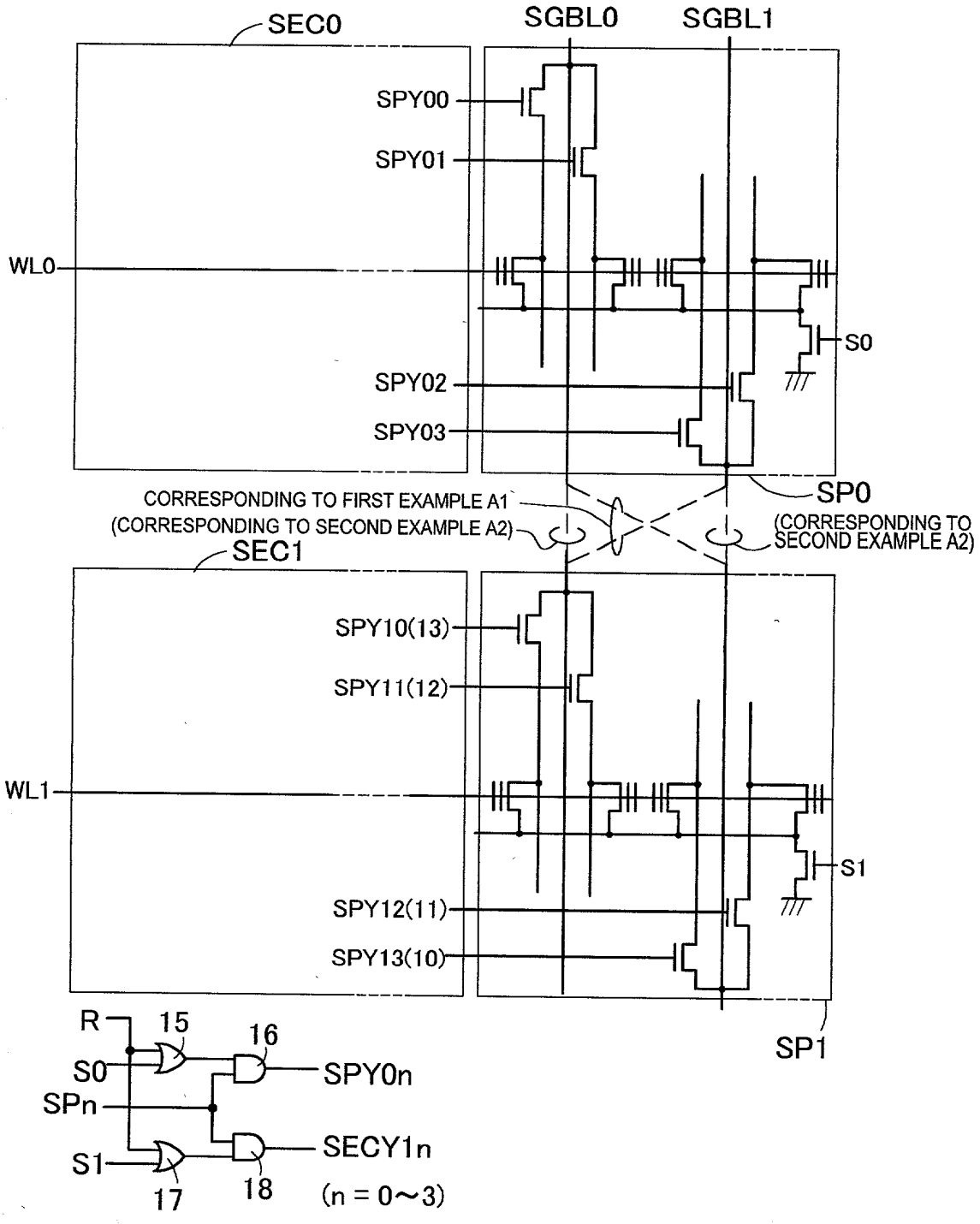


FIG.6

CIRCUIT DIAGRAM SHOWING A FIRST THEORETICAL BLOCK DIAGRAM OF A COLUMN SELECTING PORTION OF THE FIRST EMBODIMENT

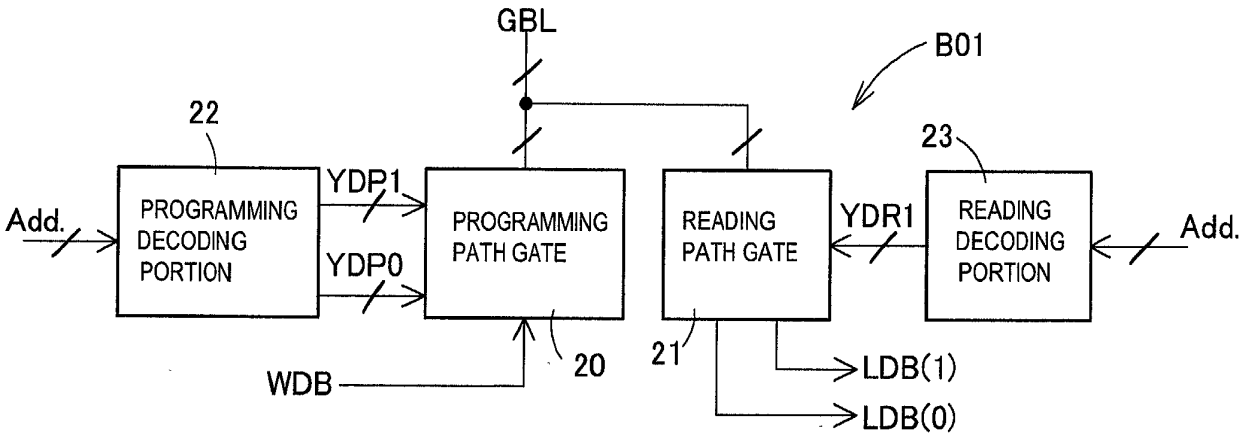


FIG.7

CIRCUIT DIAGRAM SHOWING A FIRST EXAMPLE OF THE COLUMN SELECTING PORTION

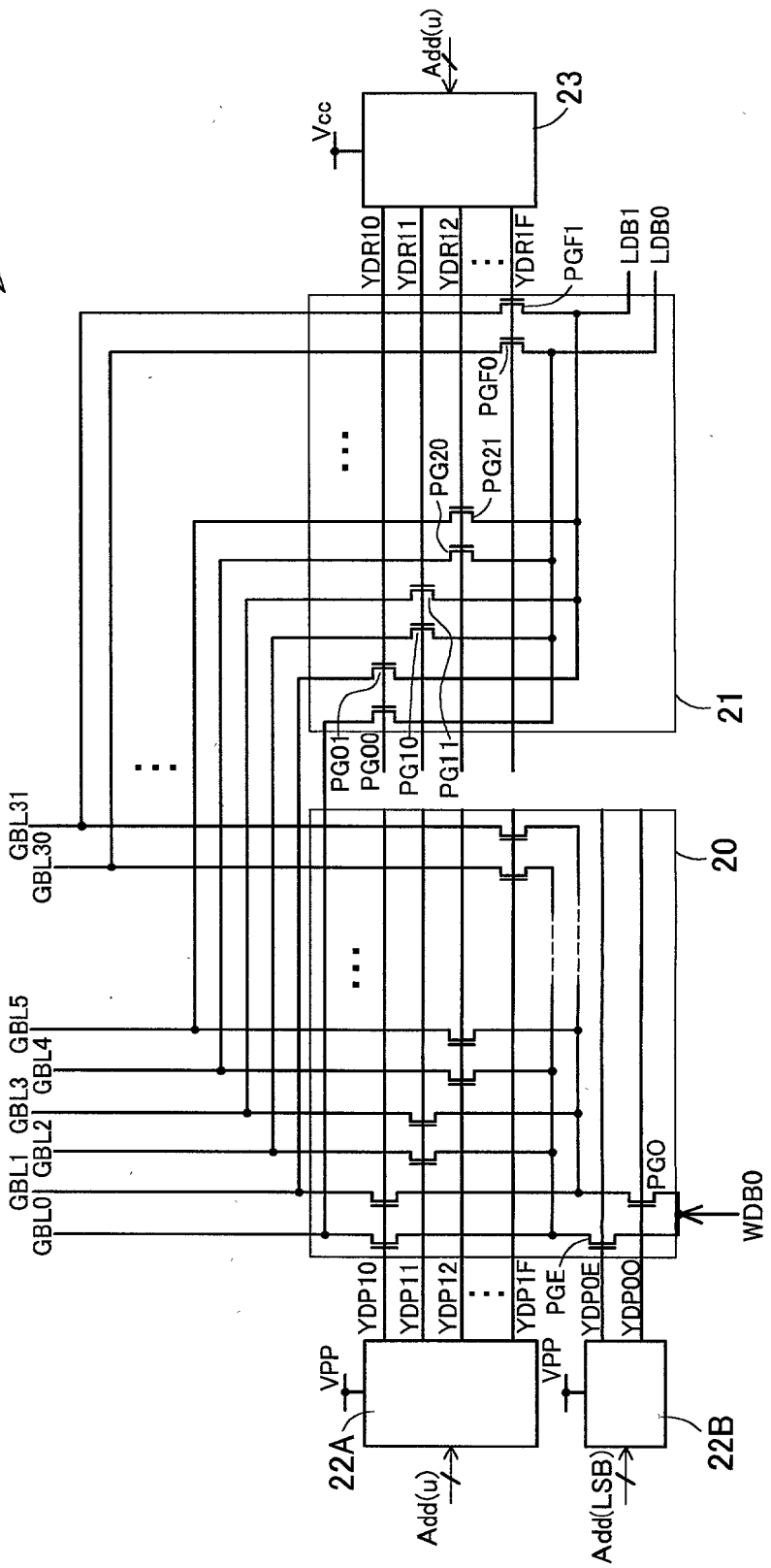


FIG.8

CIRCUIT DIAGRAM SHOWING A SECOND THEORETICAL BLOCK DIAGRAM OF THE COLUMN SELECTING PORTION OF THE FIRST EMBODIMENT

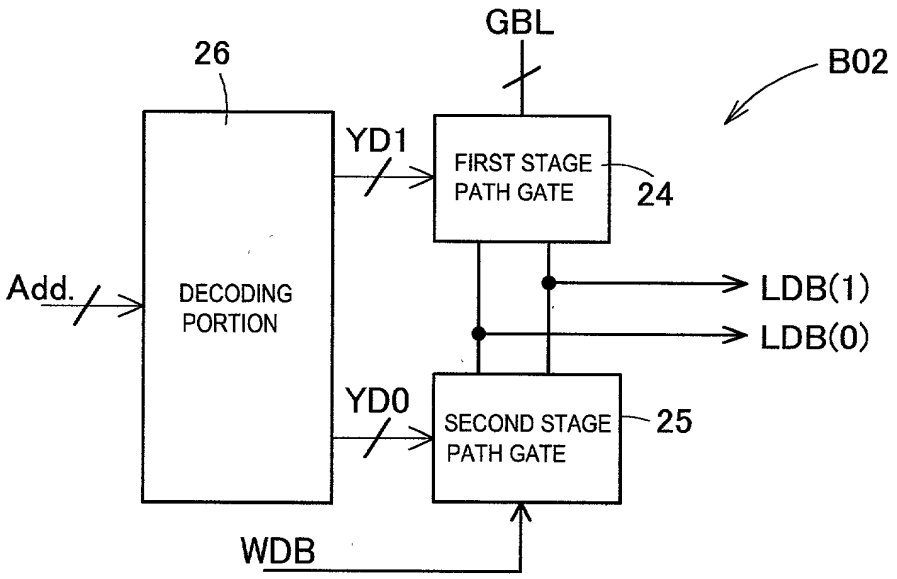


FIG.9

CIRCUIT DIAGRM SHOWING A SECOND EXAMPLE OF THE COLUMN SELECTING PORTION

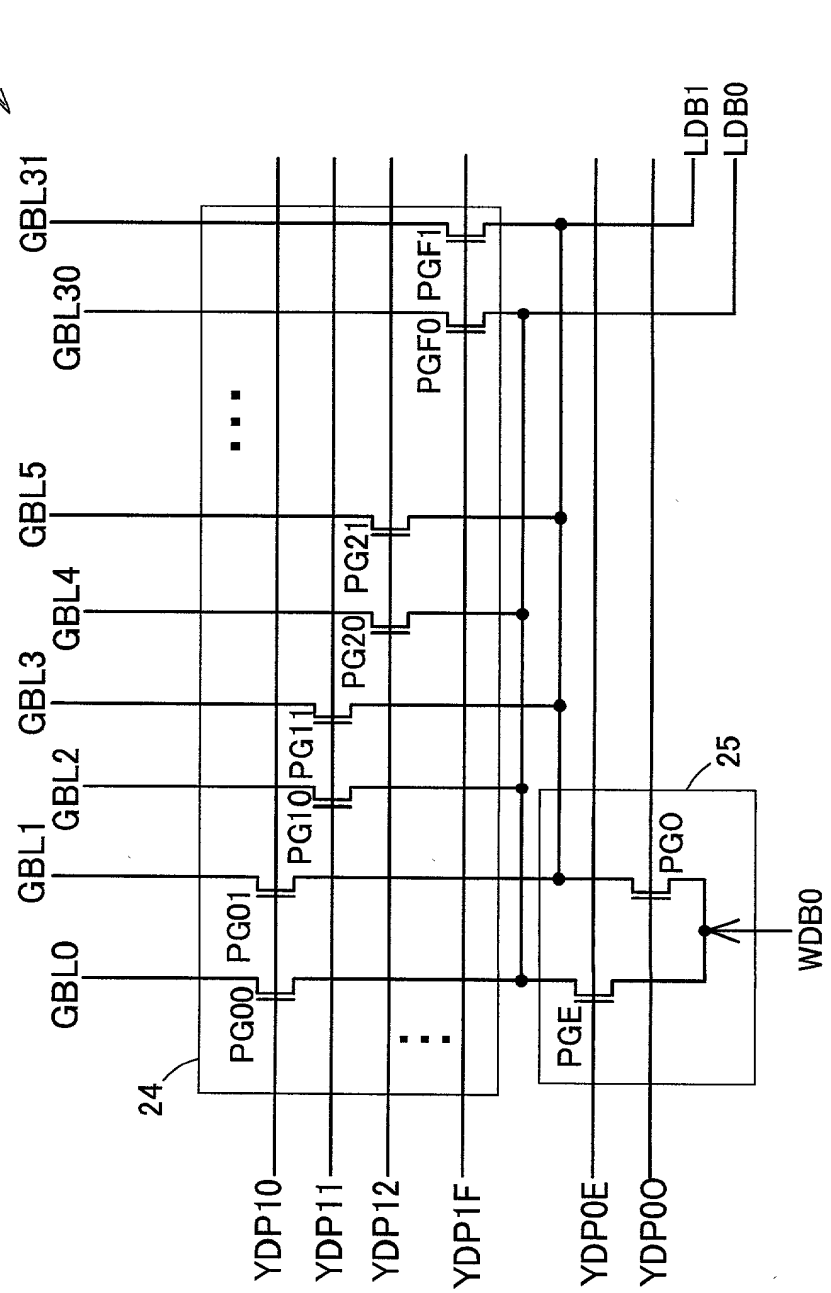


FIG.10

CIRCUIT DIAGRAM SHOWING THE FIRST THEORETICAL BLOCK DIAGRAM OF A LOADING PORTION OF THE FIRST EMBODIMENT

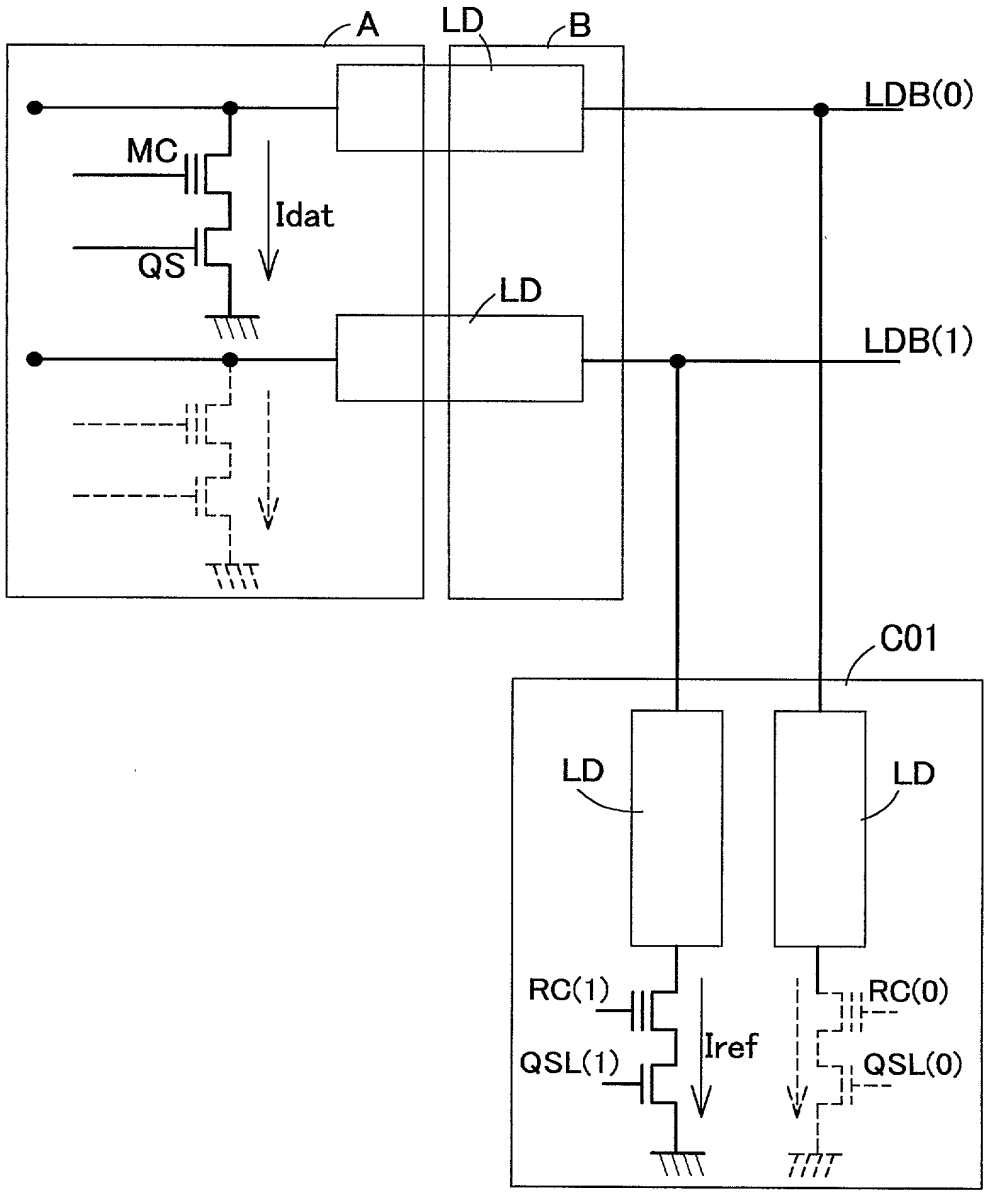
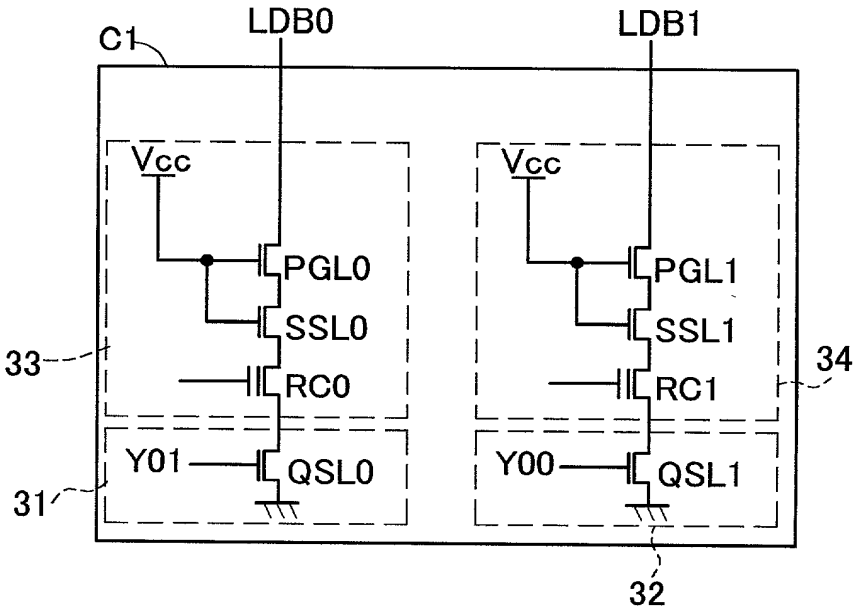


FIG.11

CIRCUIT DIAGRAM SHOWING A FIRST EXAMPLE OF THE LOADING PORTION



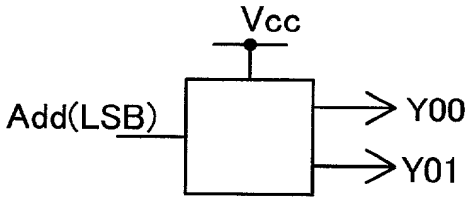


FIG.12

CIRCUIT DIAGRAM SHOWING A SECOND THEORETICAL BLOCK DIAGRAM OF A LOADING PORTION OF THE FIRST EMBODIMENT

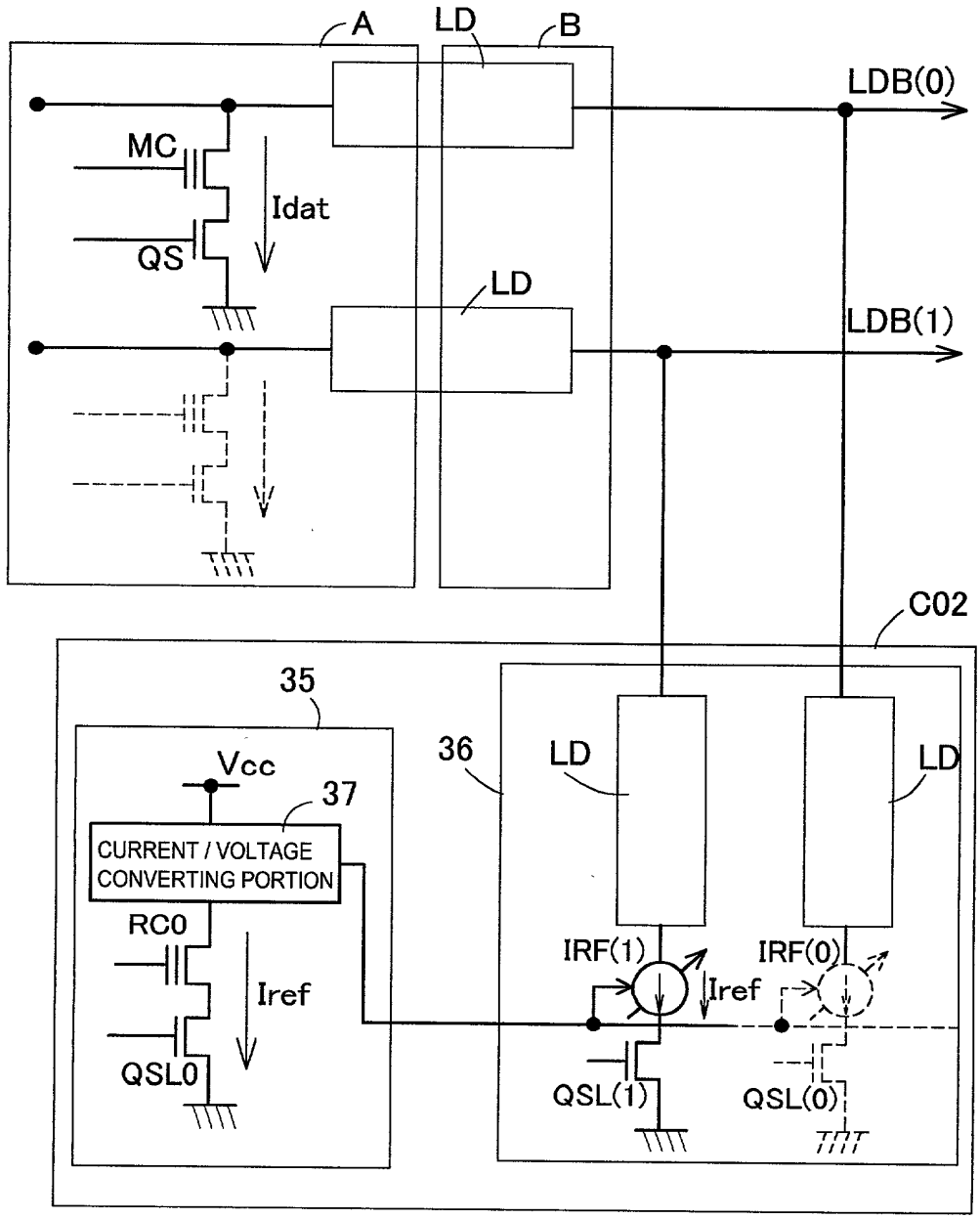


FIG.13

CIRCUIT DIAGRAM SHOWING A SECOND EXAMPLE OF THE LOADING PORTION

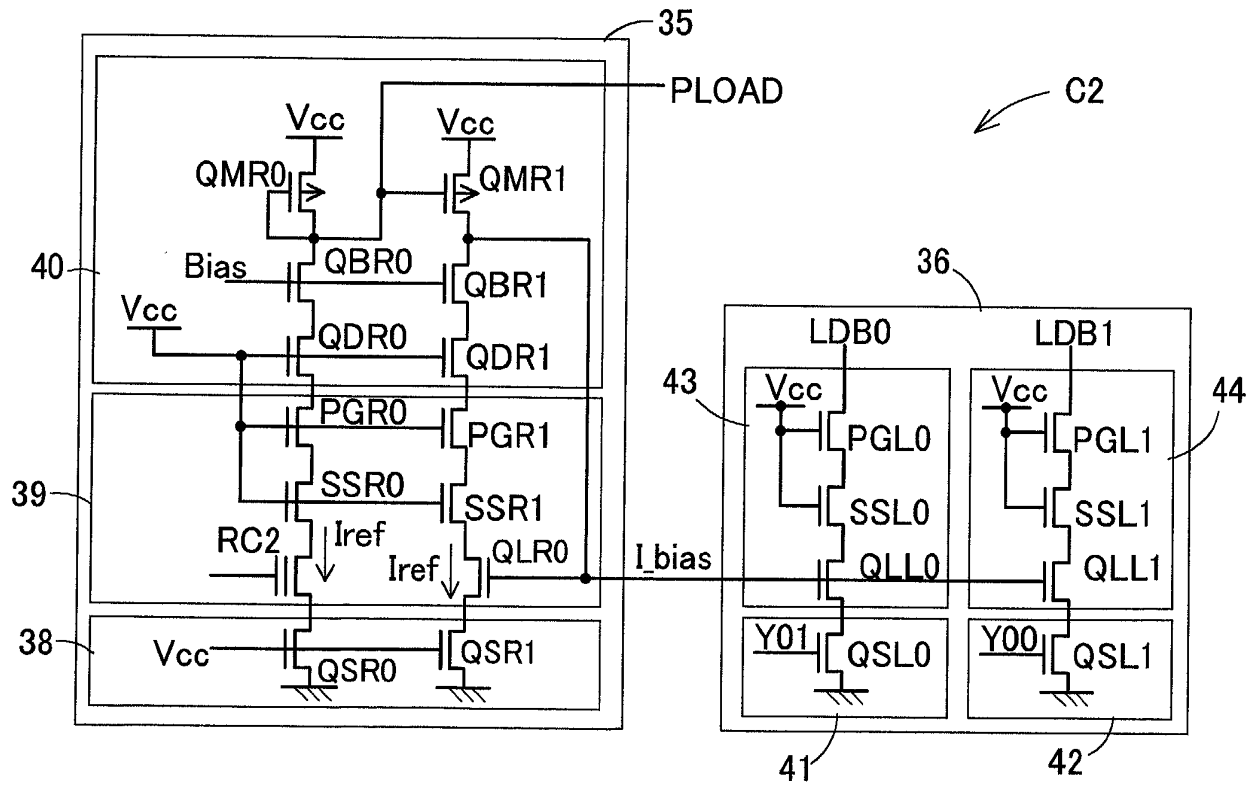


FIG.14

CIRCUIT DIAGRAM SHOWING A THIRD EXAMPLE OF THE LOADING PORTION

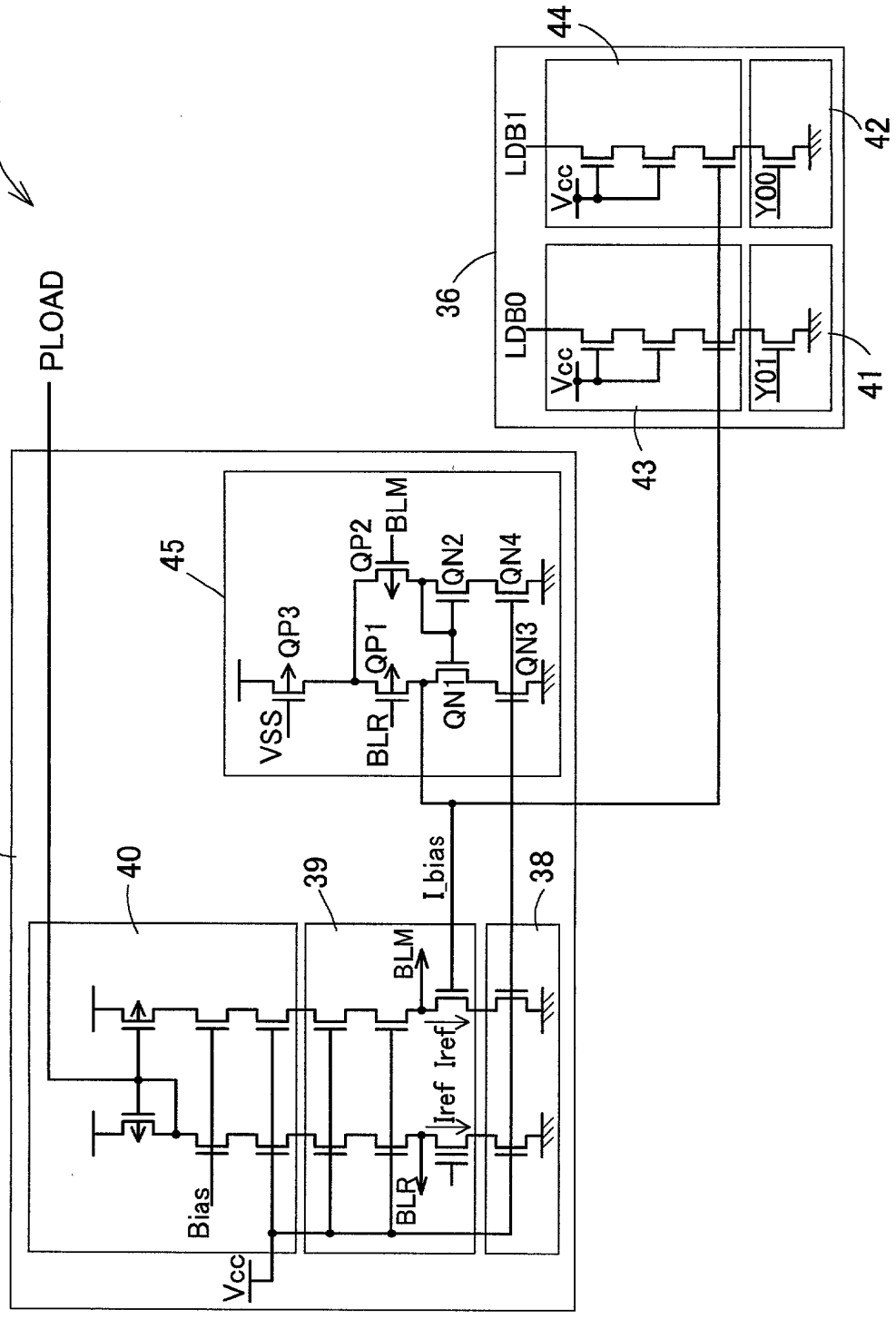


FIG.15

CIRCUIT DIAGRAM SHOWING A THEORETICAL BLOCK DIAGRAM OF A CURRENT COMPARING PORTION OF THE FIRST EMBODIMENT

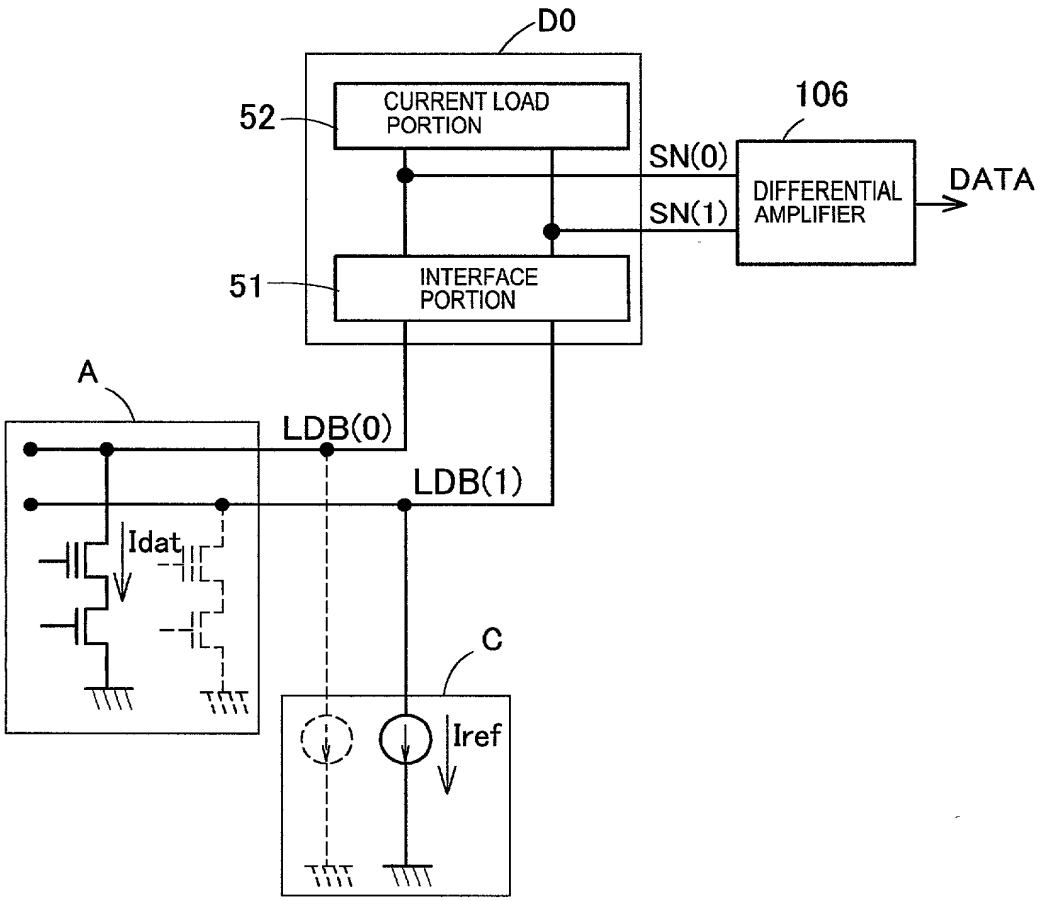


FIG.16

CIRCUIT DIAGRAM SHOWING A FIRST EXAMPLE OF THE CURRENT COMPARING PORTION

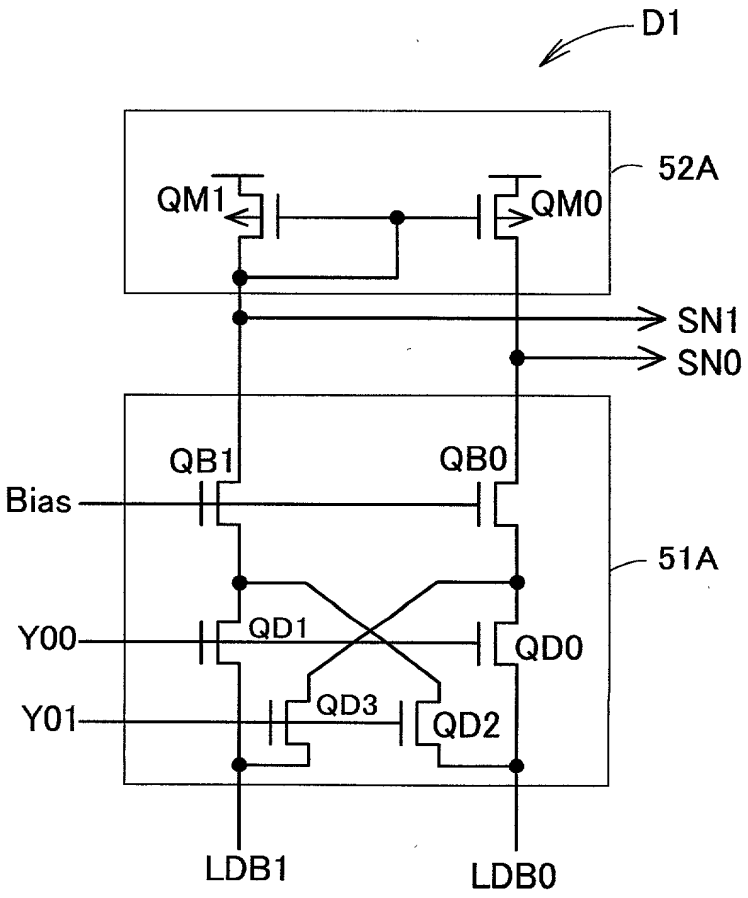


FIG.17

CIRCUIT DIAGRAM SHOWING A SECOND EXAMPLE OF THE CURRENT COMPARING PORTION

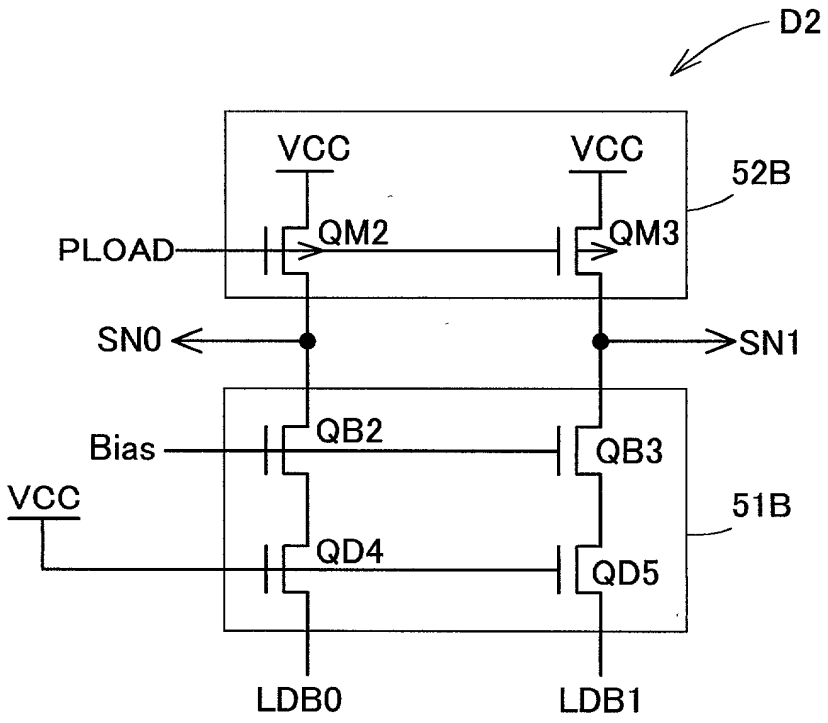


FIG.18

OPERATING WAVEFORM DIAGRAM SHOWING A READ OPERATION OF THE FIRST EMBODIMENT

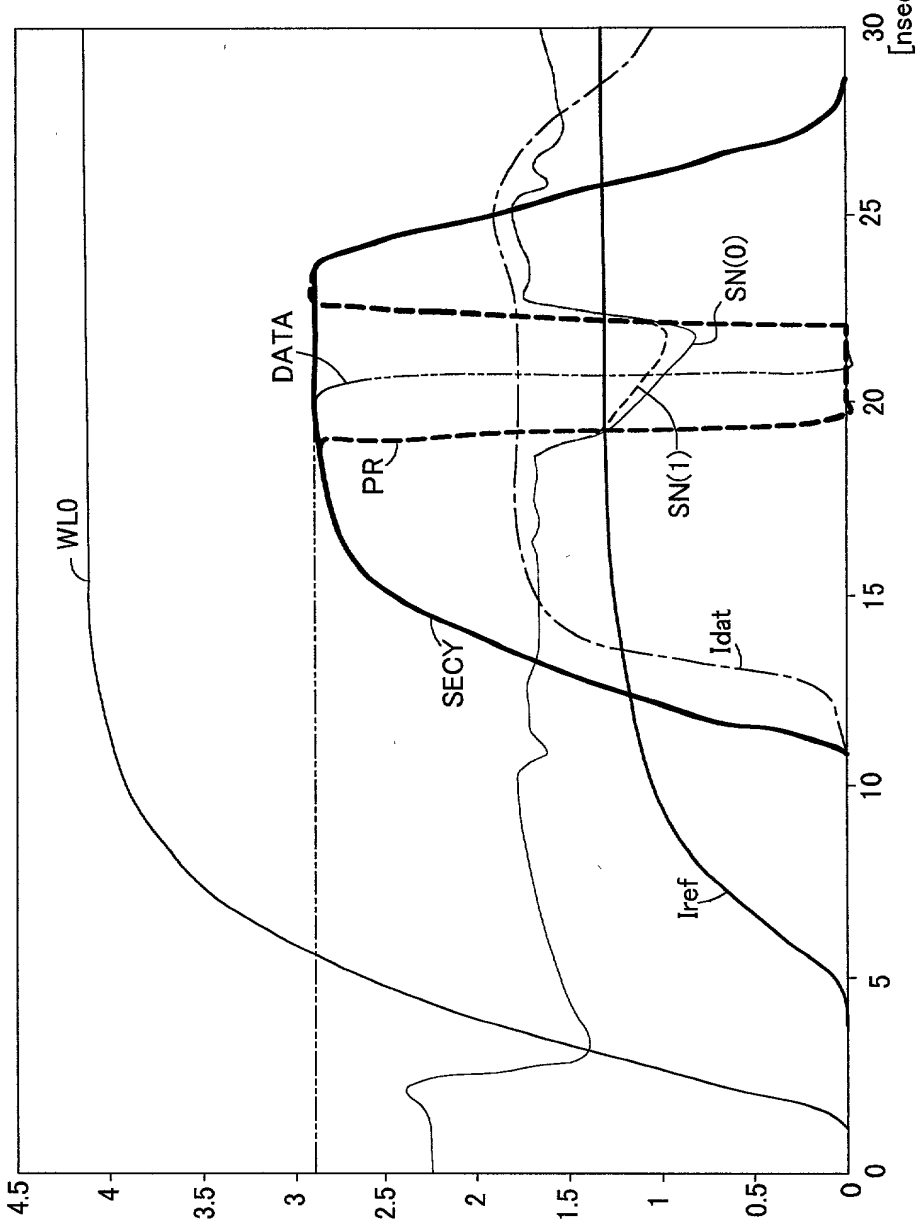


FIG.19

CIRCUIT DIAGRAM SHOWING A MEMORY CORE PORTION OF A SECOND EMBODIMENT

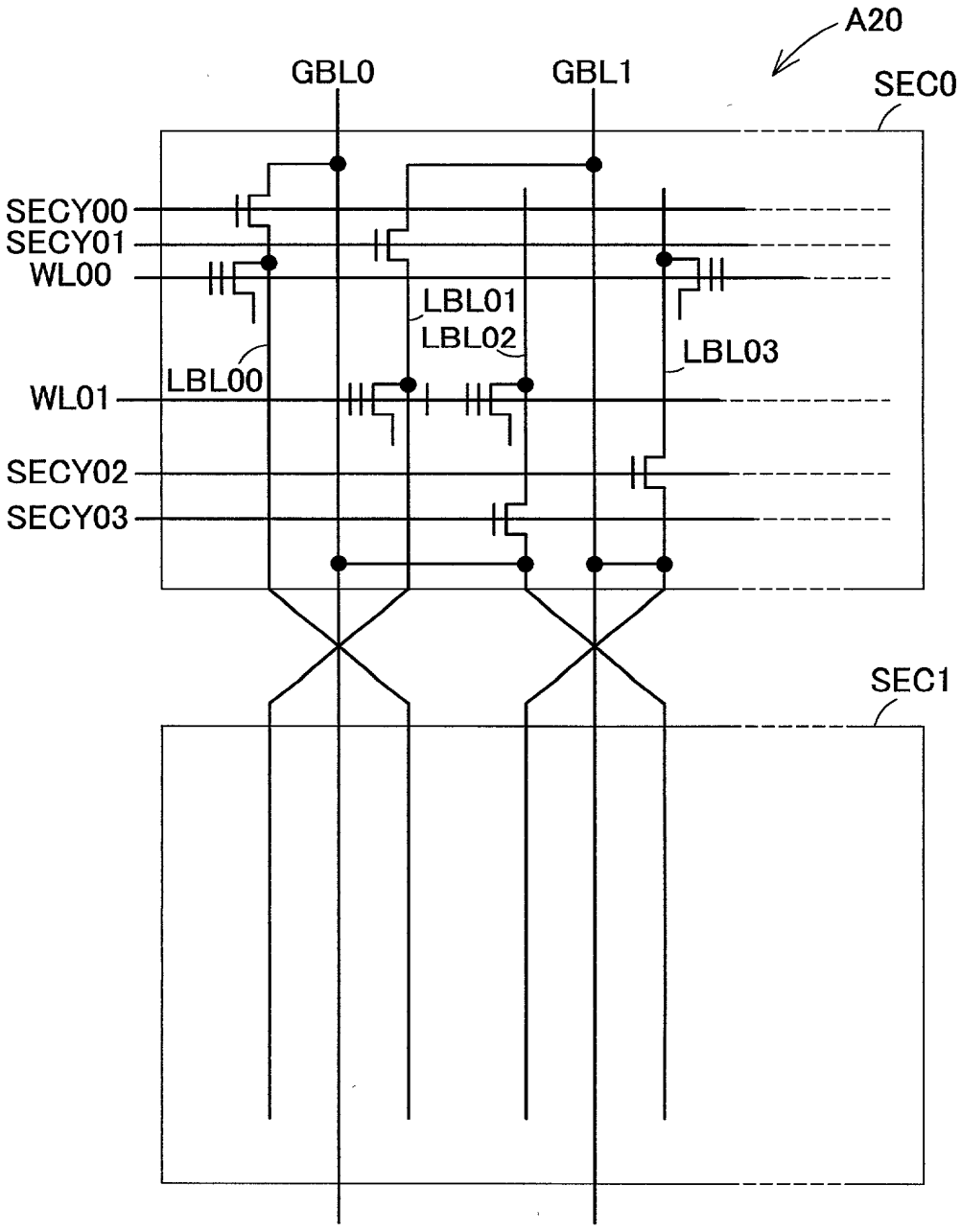


FIG.20

CIRCUIT DIAGRAM SHOWING A MEMORY CORE PORTION OF A THIRD EMBODIMENT

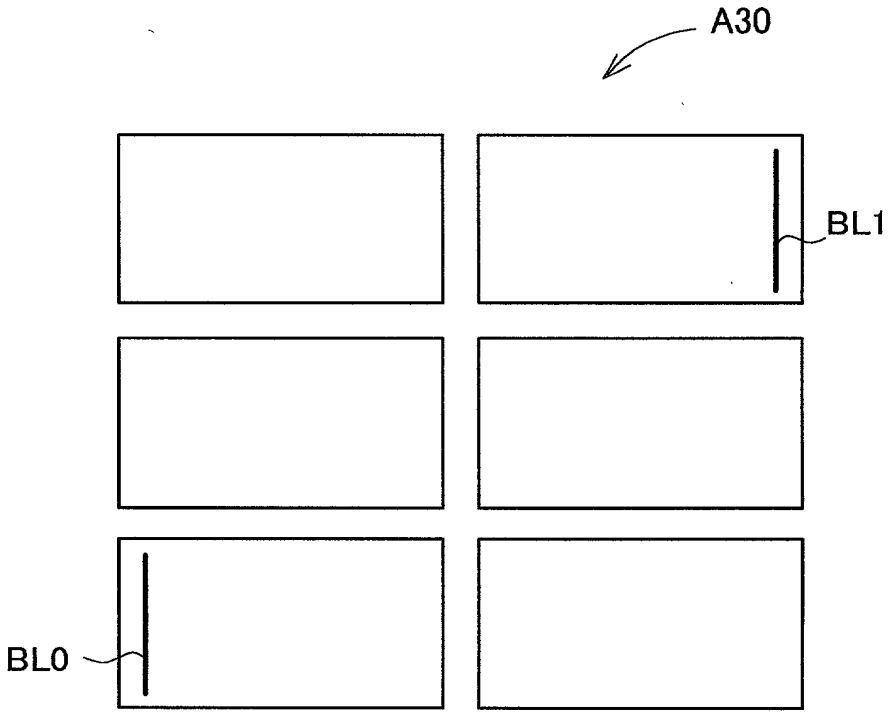


FIG.21

CIRCUIT DIAGRAM SHOWING A MEMORY CORE PORTION OF A FOURTH EMBODIMENT

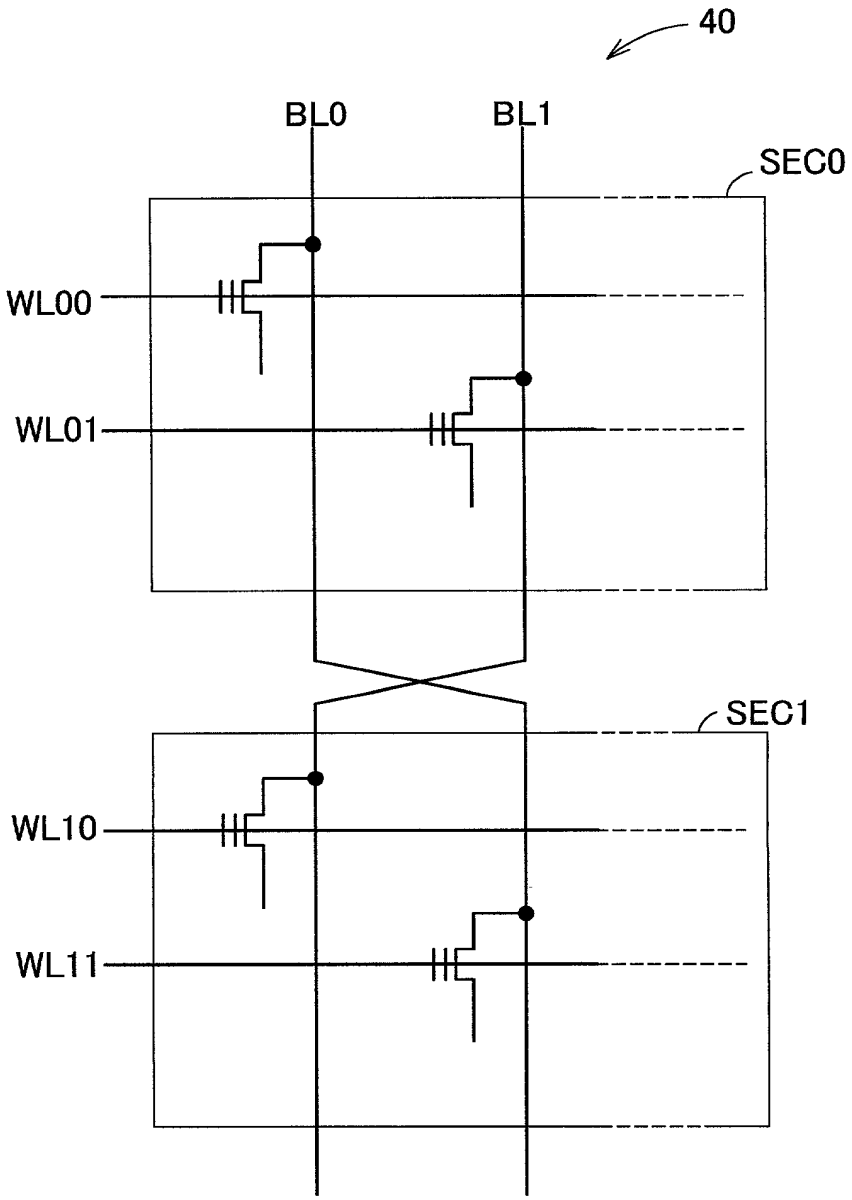


FIG.22 PRIOR ART

ENTIRE BLOCK DIAGRAM OF A CONVENTIONAL NONVOLATILE SEMICONDUCTOR MEMORY DEVICE

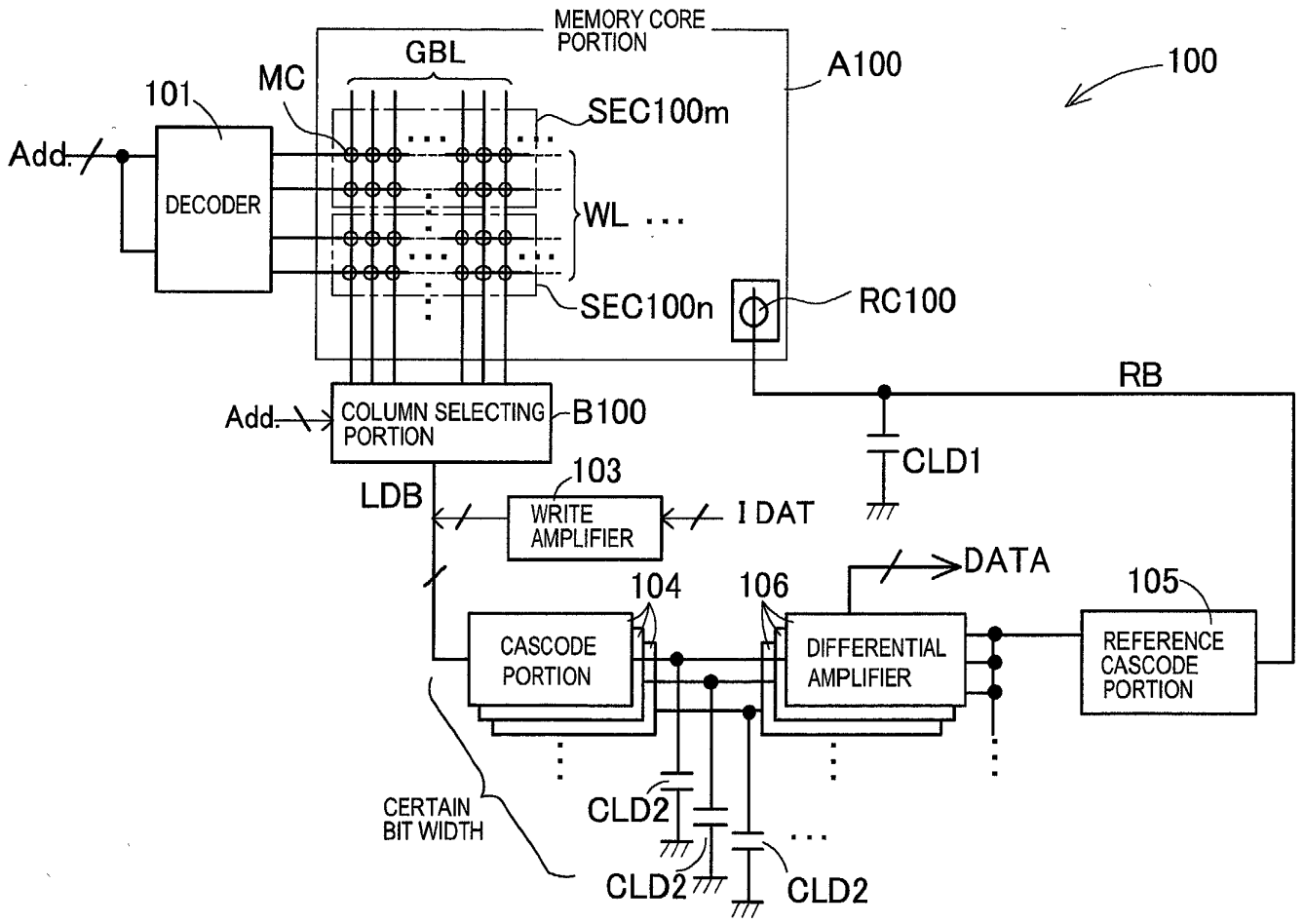


FIG.23 PRIOR ART

CIRCUIT DIAGRAM SHOWING A CONVENTIONAL MEMORY CORE PORTION

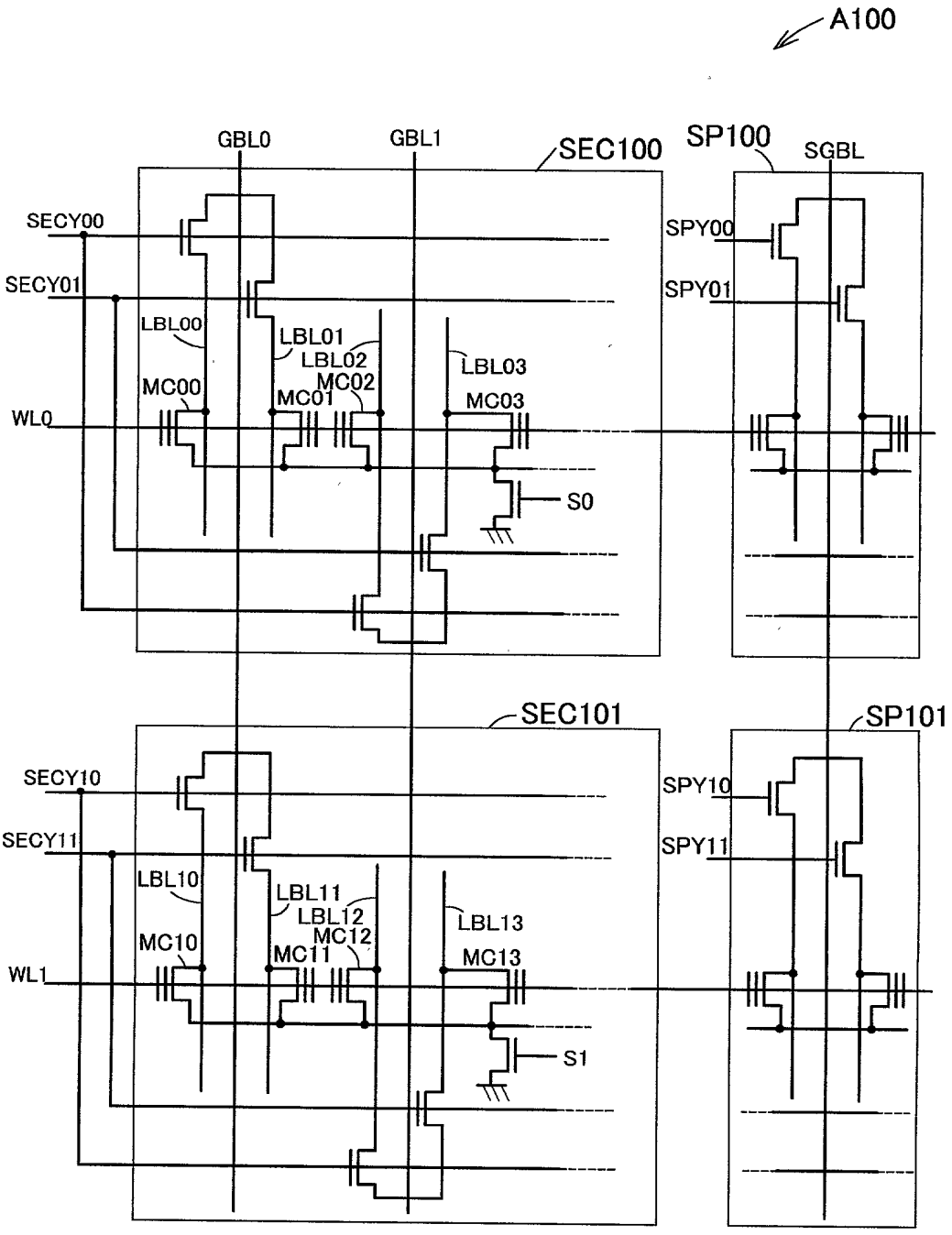


FIG.24 PRIOR ART

CIRCUIT DIAGRAM SHOWING A CONVENTIONAL COLUMN SELECTING PORTION

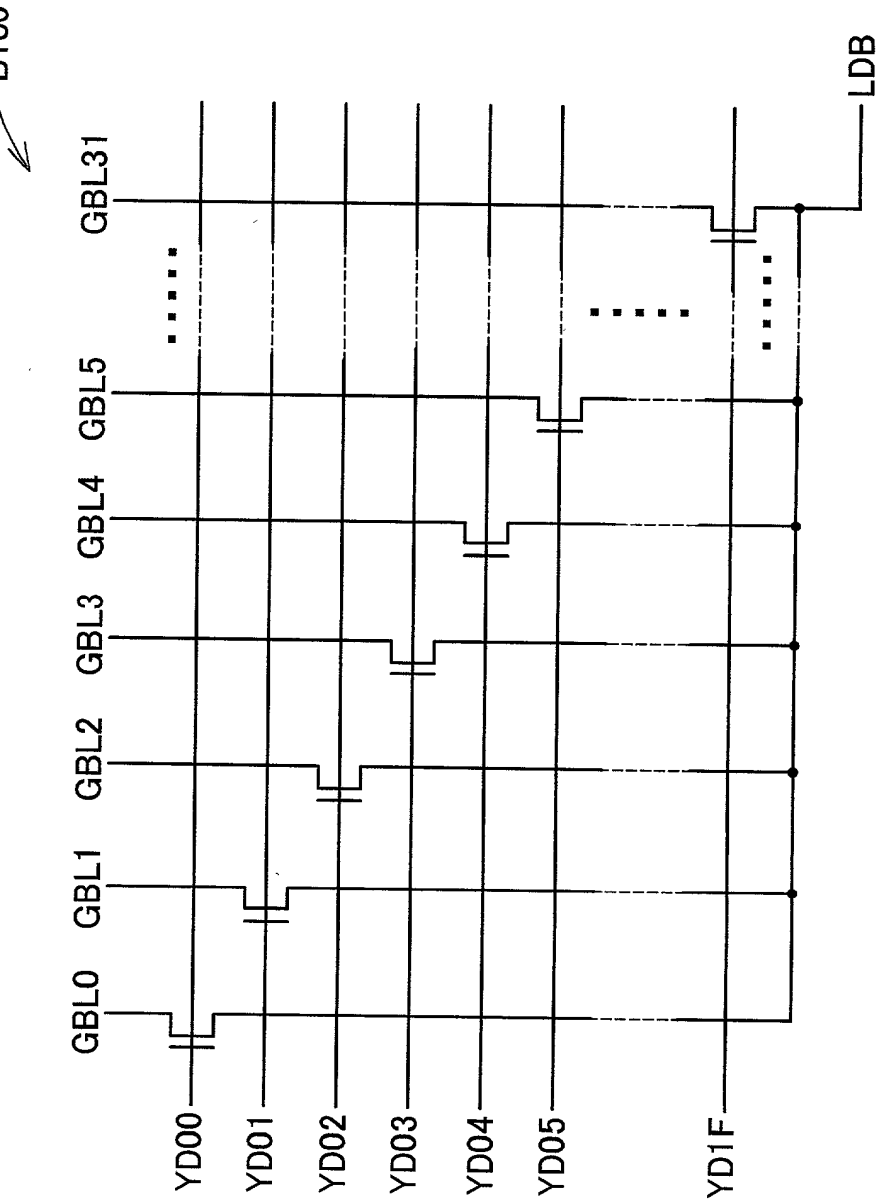


FIG.25 PRIOR ART

CIRCUIT DIAGRAM SHOWING A CONVENTIONAL COMPARING PORTION